Remarks

Claims 1-2 and 14-41 were previously presented. As a result of a restriction requirement in which claims 1-2 were held to be constructively elected by the Examiner, claims 14-41 have been withdrawn. Claims 1-2 are presented herein for Examination. Claims 1-2 have been amended herein.

Election/Restrictions

The Examiner restricted the claims to the following two groups:

Group I: Claims 1-2, directed to an integrated circuit package which includes a housing containing an integrated circuit die having at least one circuit etched thereon, the circuit comprising elements wherein negative reactive component values theoretically required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds having pre-determined inductance values, wherein the die is electrically coupled to the housing;

Group II: Claims 14-41, directed to an apparatus comprising a first inductor, a second inductor coupled to the first inductor in a shunt arrangement, and a third inductor coupled to the first inductor at a second node in a shunt arrangement.

The Examiner constructively elected the subject matter of group I, claims 1-2. As a result, claims in Group II, 14-41, have been withdrawn. The Assignee hereby intends to file a divisional application directed to Group II claims in due course. Claims 1-2 are presented herein for examination.

Claim Rejections - 35 USC § 103

The Examiner rejected claims 1-2 under 35 U.S.C. § 103(a) as being unpatentable over Busking (6,107,684) in view of Gonda (4,924,195) and Sheshita (6,366,770).

In the Examiner's rejection, the Examiner made the following statement:

> Sheshita (6,366,770) teaches (at Figs 1A, 2; col. 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein ***the theoretical values*** of the elements of the circuit required by the integrated circuit ***are actually incorporated into the circuit through the use of wire bonds 20h, 20i, 20j*** having a pre-determined inductance values, ***and wherein the wire bond inductance is used to facilitate the operation of the circuit.*** (emphasis in original)

The Assignee has carefully reviewed the passage of Sheshita cited by the Examiner, and could not find any such support or teaching as stated by the Examiner. Thus, contrary to the Examiner's assertion, the patent to Sheshita does not teach or suggest an integrated circuit package:

> wherein the negative reactive component values are actually incorporated into the circuit through the use of wire bonds having pre-determined inductance values, ***wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond***

as recited in Assignee's claim 1 as amended herein. In fact, none of the references teaches or suggests such a limitation such that neither Busking nor Gonda nor Sheshita, alone or in combination, teaches or suggests all of the elements of claim 1.

Busking merely teaches a parallel resonant circuit to tune the parasitic capacitance using a bond wire. However Busking does not teach or suggest "***wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond.***"

Gonda merely teaches realizing a negative inductance shunt arm via a SAW resonator. However, Gonda does not teach or suggest "***wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond.***"

Sheshita merely teaches a wire bond coupled to a matching circuit that has an inductor. However, Sheshita does not teach or suggest "***wherein a series inductance***

value of the integrated circuit is realized by a pre-determined inductance value of a wire bond."

Since Busking, Gonda, and Sheshita do not teach or suggest, alone or in combination, ***"wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond"***, claim 1 is not obvious in view of the patents to Busking, Gonda, and/or Sheshita, and the rejection should be withdrawn.

Furthermore, Busking, Gonda, and Sheshita do not teach or suggest, alone or in combination:

> wherein the circuit comprises an impedance inverter ***having a series inductance value, wherein the series inductance value of the impedance inverter is realized by the pre-determined inductance value of a wire bond***

as recited in claim 2 as amended herein, claim 2 is likewise not obvious in view of the patents to Busking, Gonda, and/or Sheshita. Therefore there rejection to claim 2 should be withdrawn.

It is noted that claimed subject matter may be patentably distinguished from the cited references for additional reasons; however, the foregoing is believed to be sufficient. Likewise, it is noted that the Assignee's failure to comment directly upon any of the positions asserted by the Examiner in the office action does not indicate agreement or acquiescence with those asserted positions.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested. Reconsideration of the present patent application and early allowance of all the claims is respectfully requested. Please charge any underpayments or credit any overpayments to Deposit Account No. 50-3703.

Invitation for a Telephone Interview

The Examiner is invited to call the undersigned attorney, Kenneth J. Cool, at (720) 227-9445 if there remains any issue with allowance.

Respectfully submitted,
ATTORNEY FOR ASSIGNEE

Date: _____

_____

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